NAR-ESP32S3R16/32

Edge AI · Wireless · Audio · Sensor Fusion

ESP32-S3 + 32 MB Flash + 16 MB Octal PSRAM
AXP2101 PMIC | ES8311 Codec | ES7210 Mic ADC
ICM-42670 IMU | PCF85063 RTC | 21 × 27 mm LGA-68



ADVANCE INFORMATION

This document contains preliminary technical information. Electrical characterization and certification numbers are pending bench measurements and regulatory approval. For the final pre-production revision, contact `info@corezzle.com`.

FEATURES

Processor and Memory

- Espressif ESP32-S3, Xtensa LX7 dual-core, 240 MHz
- 512 KB SRAM + 16 KB RTC SRAM (on-die)
- 16 MB Octal SPI PSRAM (on-package)
- 32 MB QSPI NOR flash (GD25LQ256, on-package)

Wireless

- Wi-Fi 4 (IEEE 802.11 b/g/n, 2.4 GHz)
- Bluetooth 5 LE + Mesh
- On-package PCB antenna or external u.FL (pin-selectable)

Power Management (AXP2101)

- Single-cell Li-Ion/LiPo charge controller
- 5 × DCDC + 4 × ALDO + 2 × BLDO rails
- I^2C control, OTP configuration
- ADC: VBAT, VBUS, TS, temperature

Audio and Sensors

- ES8311 mono I^2S codec — integrated HP driver
- ES7210 4-channel microphone ADC (TDM)
- ICM-42670-P 6-axis IMU (gyro + accel)
- PCF85063ATL I^2C RTC + 32.768 kHz

Interfaces

- USB 2.0 OTG (integrated PHY, USBLC6 ESD)
- 2 × I^2C, 3 × SPI, 3 × UART
- 2 × I^2S, LCD/Camera parallel (16-bit)
- RMII Ethernet, SDIO, TWAI (CAN), USB-JTAG
- PWM, LEDC, RMT, ADC1/2 (12-bit)

Package

- LGA-68, 21.0 × 27.0 mm, 1.9 mm height
- Castellated edge (manual or reflow assembly)
- Operating temperature: −40 °C to +85 °C **TBD** (calibration)
- RoHS compliant, Pb-free reflow profile (J-STD-020)

APPLICATIONS

- Wearable devices (smartwatch, fitness band)
- Voice IoT assistants, smart speakers
- Industrial data acquisition (DAQ)
- Vehicle telematics and asset tracking
- Building automation, smart thermostats
- Medical monitors and patient tracking (non-certified)
- Robotic sensor fusion
- Mesh network edge nodes
- Battery-powered edge AI inference

DEVELOPMENT ECOSYSTEM

- Open-source development kit (Apache-2.0)
- ESP-IDF, Arduino-ESP32, MicroPython support
- Multiple RTOS examples: FreeRTOS, Zephyr, NuttX
- Reference applications: smartwatch, vehicle tracker, home automation
- GitLab CI manufacturing test firmware
- Repo: `github.com/CorezzleElectronics/nar-esp32s3-devkit`

PART INFORMATION

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Contents

1 Product Overview **1**
- 1.1 Product Description . . . 1
- 1.2 Target Markets . . . 1
- 1.3 Key Advantages . . . 1
- 1.4 About This Document . . . 2
  - 1.4.1 Document Structure . . . 2
  - 1.4.2 Document Status . . . 2

2 Block Diagram and Internal Architecture **3**
- 2.1 System Block Diagram . . . 3
- 2.2 On-Package ICs . . . 3
- 2.3 Inter-Chip Connectivity . . . 3
  - 2.3.1 Data Buses . . . 3
  - 2.3.2 Interrupt and Control Lines . . . 4
- 2.4 Power Architecture (Summary) . . . 4

3 Pin Configuration and Functions **6**
- 3.1 Package Pinout . . . 6
- 3.2 Pin Function Table . . . 6
- 3.3 Pin Category Summary . . . 8
- 3.4 ESP32-S3 GPIO ↔ SiP Pin Matrix . . . 8
- 3.5 Unconnected / Invisible GPIOs . . . 8

4 Electrical Characteristics **11**
- 4.1 Absolute Maximum Ratings . . . 11
- 4.2 Recommended Operating Conditions . . . 11
- 4.3 DC Characteristics . . . 11
- 4.4 Power Consumption . . . 12
- 4.5 Reset and Power-Up Sequencing . . . 12
  - 4.5.1 Power-Up Sequence . . . 12
  - 4.5.2 Manual Reset . . . 13
  - 4.5.3 Brown-Out Detection . . . 13

5 RF Characteristics **14**
- 5.1 Wi-Fi (IEEE 802.11 b/g/n) . . . 14
  - 5.1.1 General Specifications . . . 14
  - 5.1.2 TX Output Power (Manufacturer nominal values) . . . 14
  - 5.1.3 RX Sensitivity . . . 15
- 5.2 Bluetooth 5 LE + Mesh . . . 15
  - 5.2.1 General Specifications . . . 15
  - 5.2.2 TX Output Power . . . 15
  - 5.2.3 RX Sensitivity . . . 15
- 5.3 Antenna Options . . . 16
  - 5.3.1 On-Package PCB Antenna . . . 16
  - 5.3.2 External u.FL / IPEX MHF1 . . . 16
- 5.4 Regulatory Certification Status . . . 16

6 On-Package Peripherals **18**
6.1 Audio Codec — ES8311 . . . 18
6.1.1 SiP Integration . . . 18
6.1.2 Performance Summary (Manufacturer nominal) . . . 18
6.2 Microphone ADC — ES7210 . . . 18
6.2.1 SiP Integration . . . 19
6.2.2 Performance Summary (Manufacturer nominal) . . . 19
6.3 IMU — ICM-42670-P . . . 20
6.3.1 SiP Integration . . . 20
6.3.2 Performance Summary (Manufacturer nominal) . . . 20
6.4 RTC — PCF85063ATL . . . 20
6.4.1 SiP Integration . . . 21
6.4.2 Performance Summary (Manufacturer nominal) . . . 21
6.5 Flash Memory — GD25LQ256DWIGR . . . 21
6.5.1 SiP Integration . . . 21
6.5.2 Performance Summary . . . 21
6.6 USB-C ESD Protection — USBLC6-2SC6 . . . 22

7 Power Management and Distribution **23**
7.1 AXP2101 PMIC — Overview . . . 23
7.2 Input Specifications . . . 23
7.3 Rail Specifications . . . 23
7.3.1 Rail Performance . . . 24
7.4 Charge Control . . . 24
7.5 Power-Path . . . 24
7.6 ADC Channels . . . 24
7.7 Power-Up Sequencing . . . 25

8 Boot and Programming **26**
8.1 Boot Flow . . . 26
8.2 Strap Pins . . . 26
8.3 Download Mode (Programming) . . . 26
8.3.1 Automatic Download . . . 26
8.3.2 Manual Download . . . 27
8.4 USB-Serial-JTAG . . . 27
8.5 eFuse Configuration . . . 27
8.6 Security Features . . . 28
8.6.1 Secure Boot v2 . . . 28
8.6.2 Flash Encryption . . . 28
8.6.3 HMAC and Digital Signature Peripherals . . . 28
8.7 Programming Flow . . . 28

9 Mechanical Information **29**
9.1 Package Overview . . . 29
9.2 Package Dimensions (Nominal) . . . 29
9.3 Pad Geometry . . . 29
9.4 Mechanical Drawing . . . 30
9.5 Recommended Land Pattern (IPC-7351B) . . . 30
9.6 Tape & Reel Information . . . 30
9.7 Reflow Profile . . . 31
9.7.1 Reflow Tolerance of On-Package Chips . . . 31
9.7.2 Solder Flux Selection . . . 32
9.8 Moisture Sensitivity Level (MSL) . . . 32
9.9 ESD Handling . . . 32

10 Application Information **36**
10.1 Reference Design . . . 36
10.2 Power — External BoM . . . 36
10.3 Antenna Placement Guidelines . . . 37
10.3.1 On-Package PCB Antenna (Default) . . . 37
10.3.2 External u.FL / IPEX MHF1 . . . 37
10.4 Decoupling Strategy . . . 37
10.5 Thermal Considerations . . . 37
10.6 EMI / EMC Guidance . . . 38
10.7 Software Development . . . 38

11 Ordering Information **39**
11.1 Available Part Numbers . . . 39
11.2 Part Number Structure . . . 39
11.3 Samples and Evaluation . . . 39
11.3.1 Engineering Samples . . . 39
11.3.2 Development Kit . . . 40
11.4 Lead Time . . . 40
11.5 Quality and Test . . . 40
11.6 Warranty . . . 41

12 Revision History **42**
12.1 Revision Table . . . 42
12.2 Revision Levels . . . 42
12.3 Expected in the Next Revision . . . 42
12.4 Update Notification . . . 43

13 Legal and Compliance **44**
13.1 Disclaimer . . . 44
13.2 Validity of Information . . . 44
13.3 Warranty . . . 44
13.4 Industry Standards . . . 44
13.5 Regulatory Conformity . . . 44
13.6 Intellectual Property . . . 44
13.7 Use Limitation . . . 44
13.8 Right to Change . . . 45
13.9 Third-Party Chips . . . 45
13.10 Patent and License Notices . . . 45
13.11 Export Control . . . 45
13.12 Recycling and RoHS . . . 45
13.13 Contact . . . 45

14 Upstream Datasheets **46**
14.1 Chip Datasheets . . . 46
14.2 Related Espressif Documents . . . 47
14.3 Standards and Regulations . . . 47
14.4 Corezzle Documents . . . 47

CHAPTER 1

Product Overview

1.1 Product Description

NAR-ESP32S3R16/32, manufactured by Corezzle Elektronik A.Ş., is a fully-functional **System-in-Package (SiP)** solution housed in a 21 × 27 mm LGA-68 package. The package integrates the Espressif ESP32-S3 processor, 16 MB octal SPI PSRAM, 32 MB QSPI flash, the X-Powers AXP2101 PMIC, and a peripheral chip set calibrated for wearable / IoT applications (audio codec, microphone ADC, IMU, RTC and USB ESD protection) into a single package.

While delivering functional density roughly equivalent to a carrier module, the device is supplied under a single part number with SiP-level RF calibration, optimized power distribution and factory-grade testing. This removes the burden of RF certification, power-tree validation and EMI/EMC compensation from the development team consuming the part.

1.2 Target Markets

NAR-ESP32S3R16/32 is designed as a general-purpose wireless edge node and is particularly suited for direct use in the following classes:

- Wearable devices (smartwatch, fitness band, health monitor)
- Voice IoT — smart speakers, voice command interfaces
- Vehicle telematics and asset tracking
- Industrial sensor / data acquisition (DAQ)
- Building automation — thermostats, smart outlets, gateways
- Battery-powered edge AI inference (TensorFlow Lite Micro, ESP-NN, leveraging on-package PSRAM)

1.3 Key Advantages

Single-package integration
Beyond what Espressif modules (ESP32-S3-WROOM-1) offer, audio, sensors, RTC and power management are fully integrated. The external BoM is reduced to the antenna, USB connector, battery and, where required, microphone/speaker.

On-package PMIC
The AXP2101 handles the system-wide power tree with Li-Ion/LiPo charge control, five DCDCs and six LDO rails. No external charge IC or rail partitioning is needed.

Development ecosystem
Delivered with an Apache-2.0 licensed open-source development kit, ESP-IDF reference applications (smartwatch, vehicle tracker, home automation) and multi-RTOS examples (FreeRTOS, Zephyr, NuttX).

Production-ready
Castellated LGA edges support both manual prototyping and pick-and-place SMT flows. Compatible with the J-STD-020 reflow profile.

1.4 About This Document

This datasheet does not reproduce the full electrical datasheet of every on-package chip; instead, it details the *SiP-specific* electrical, mechanical and application parameters. The official manufacturer datasheet for each chip is referenced as the *upstream source* (see chapter 14), giving direct access to the most current and authoritative technical information.

1.4.1 Document Structure

Table 1.1. Datasheet chapters and reader guide.

Chapter	Title	Target Reader / Content
2	Block Diagram	Reader requiring a quick grasp of the system architecture
3	Pin Configuration	PCB designer, software developer — 68-pin function and GPIO matrix
4	Electrical	Hardware designer — AbsMax, RecOp, DC, power consumption
5	RF	RF engineer, certification officer — Wi-Fi/BLE, antenna
6	Peripherals	Software developer — I^2C addresses, performance specs
7	Power Management	Hardware designer — AXP2101 rails, charging, ADC
8	Boot and Programming	Software developer — strap pins, eFuse, security
9	Mechanical	PCB designer, manufacturing — package dimensions, land pattern, reflow
10	Application Information	System designer — reference circuit, decoupling, antenna layout
11	Ordering Information	Procurement — PN, samples, lead-time
12–14	Revision / Legal / Upstream Sources	—

1.4.2 Document Status

This document is at Rev. 0.1 ADVANCE INFORMATION status. Electrical characterization (bench measurements), certification numbers (CE, FCC, BLE SIG, Wi-Fi Alliance) and the final mechanical drawings are still in progress as part of the product development cycle. Fields marked with **TBD** will be filled in during the final pre-production revision. For revision levels and the next-revision plan, see chapter 12.

CHAPTER 2

Block Diagram and Internal Architecture

2.1 System Block Diagram

Figure 2.1 shows the on-package signal flow of NAR-ESP32S3R16/32. All chips are powered through rails generated by the AXP2101 PMIC; the ESP32-S3 acts as the system main controller.

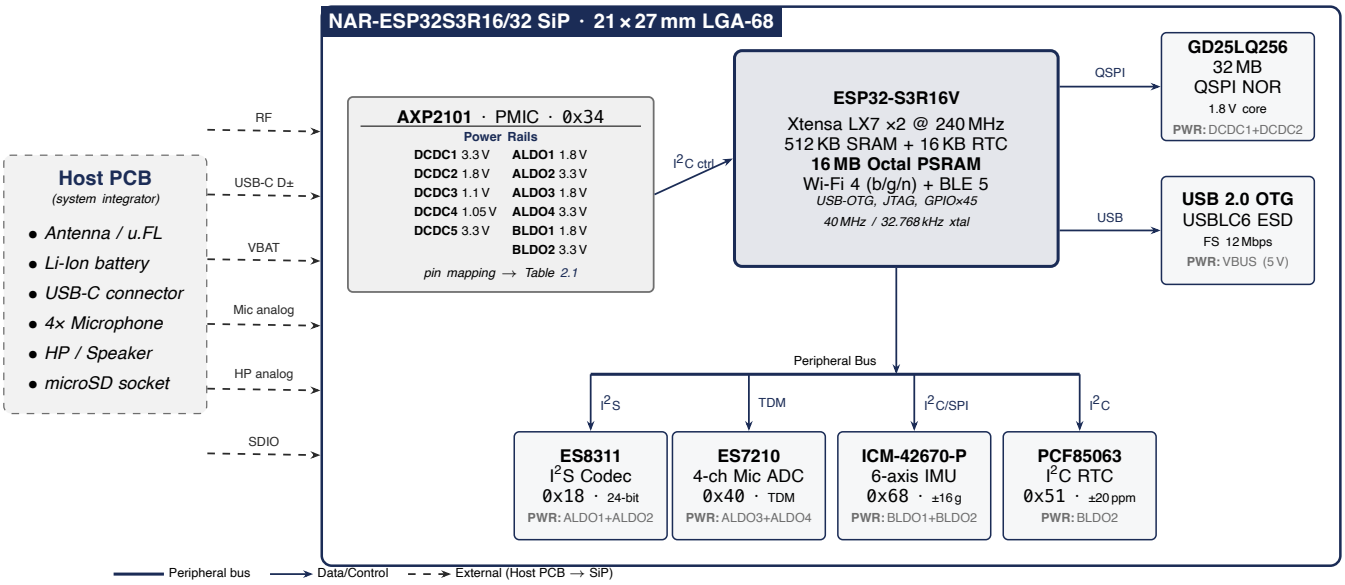

Figure 2.1. NAR-ESP32S3R16/32 system block diagram. The bold bus bar denotes shared peripheral interfaces, thin arrows show point-to-point data/control lines, dashed grey arrows show Host PCB connections. I^2C addresses appear beneath each block in 7-bit hex format. The PMIC rail map is detailed in Table 2.1.

2.2 On-Package ICs

The following table lists all active devices integrated within the SiP. The full electrical datasheet of each chip is available from the manufacturer's official sources (chapter 14).

2.3 Inter-Chip Connectivity

2.3.1 Data Buses

- **I^2C_0 (system):** ESP32-S3 ↔ AXP2101, ICM-42670, PCF85063, ES8311, ES7210. Pull-ups are on-package (3.3 V rail).
- **I^2S_0 (audio out):** bi-directional speaker/HP streaming via ES8311.
- **TDM (audio in):** 4-channel microphone stream via ES7210; optional shared bit clock with ES8311.

Table 2.1. AXP2101 PMIC power rail map. Each rail's nominal voltage, maximum current capability and supplied IC + pin name. DCDC rails feed high-current digital domains, ALDO rails feed analog islands, BLDO rails feed bypass-mode low-noise blocks. UVLO thresholds and sequencing details are in chapter 7.

Rail	Voltage	Max. current	Supplied blocks (IC + pin)
DCDC (high-current step-down converters)			
DCDC1	3.3 V	2.0 A	ESP32-S3 `VDD3P3` + GD25LQ256 `VCC` + ICM-42670 `VDDIO` + PCF85063 `VDD` + sensor IO
DCDC2	1.8 V	2.0 A	ESP32-S3 `VDD_SPI` (1.8 V flash low-power mode) — or reserve
DCDC3	1.1 V	2.0 A	ESP32-S3 `VDDA_1P1` (CPU core boost, shared with internal LDO)
DCDC4	1.05 V	1.5 A	Reserve (expandable core voltage domain)
DCDC5	3.3 V	1.0 A	Reserve (sensor analog island / external peripheral)
ALDO (analog LDOs, audio/sensor analog islands)			
ALDO1	1.8 V	300 mA	ES8311 `DVDD` (codec digital island)
ALDO2	3.3 V	300 mA	ES8311 `AVDD` + `MVDD` (codec analog + HP driver)
ALDO3	1.8 V	300 mA	ES7210 `DVDD` (mic ADC digital island)
ALDO4	3.3 V	300 mA	ES7210 `AVDD` (mic ADC analog island)
BLDO (bypass LDOs, low-noise sensor islands)			
BLDO1	1.8 V	300 mA	ICM-42670-P `VDDIO` (IMU digital interface, dropout-aware)
BLDO2	3.3 V	300 mA	ICM-42670-P `RVDD` + PCF85063 `VBAT` (sensor analog + RTC backup)

Table 2.2. NAR-ESP32S3R16/32 on-package chip list.

Chip	Manufacturer	Function	Interface
ESP32-S3R16V	Espressif	Dual-core LX7 MCU + 16 MB octal PSRAM + Wi-Fi/BLE	SoC
GD25LQ256DWIGR	GigaDevice	32 MB QSPI NOR flash	QSPI
AXP2101	X-Powers	Multi-rail PMIC + Li-Ion charging	I^2C
ES8311	Everest Semi	Mono I^2S audio codec + HP	I^2S + I^2C
ES7210	Everest Semi	4-channel microphone ADC (TDM)	TDM + I^2C
ICM-42670-P	TDK InvenSense	6-axis IMU (gyro + accel)	I^2C/SPI
PCF85063ATL	NXP	I^2C RTC + 32.768 kHz oscillator	I^2C
USBLC6-2SC6	ST	USB-C ESD protection (TVS)	USB D+/D–

- **QSPI (flash):** GD25LQ256 connected to the ESP32-S3 integrated QSPI flash interface (calibrated).
- **USB 2.0:** ESP32-S3 internal PHY, brought outside the package through USBLC6.

2.3.2 Interrupt and Control Lines

The INT pins of ICM-42670, PCF85063 and AXP2101 connect to GPIO inputs of the ESP32-S3, allowing every peripheral to provide event-driven wake-up in low-power modes. For detailed pin assignment, see chapter 3.

2.4 Power Architecture (Summary)

The AXP2101 accepts power from USB VBUS (5 V) or a single-cell Li-Ion (3.0–4.2 V) input and generates the system rails:

- **DCDC1**: 3.3 V system rail (ESP32-S3, flash, IMU, RTC)
- **DCDC2–5**: user-configurable auxiliary rails

- **ALDO1–4, BLDO1–2**: analog/digital island supplies, per-peripheral LDOs

Full rail mapping and current capacities are given in chapter 7.

CHAPTER 3

Pin Configuration and Functions

3.1 Package Pinout

Figure 3.1 shows the top view of the 68-pin LGA package drawing. Pads are on the bottom of the package; the drawing is rendered transparent for clarity. Pin 1 is in the top-left corner (red marker). Pin numbering advances counter-clockwise.

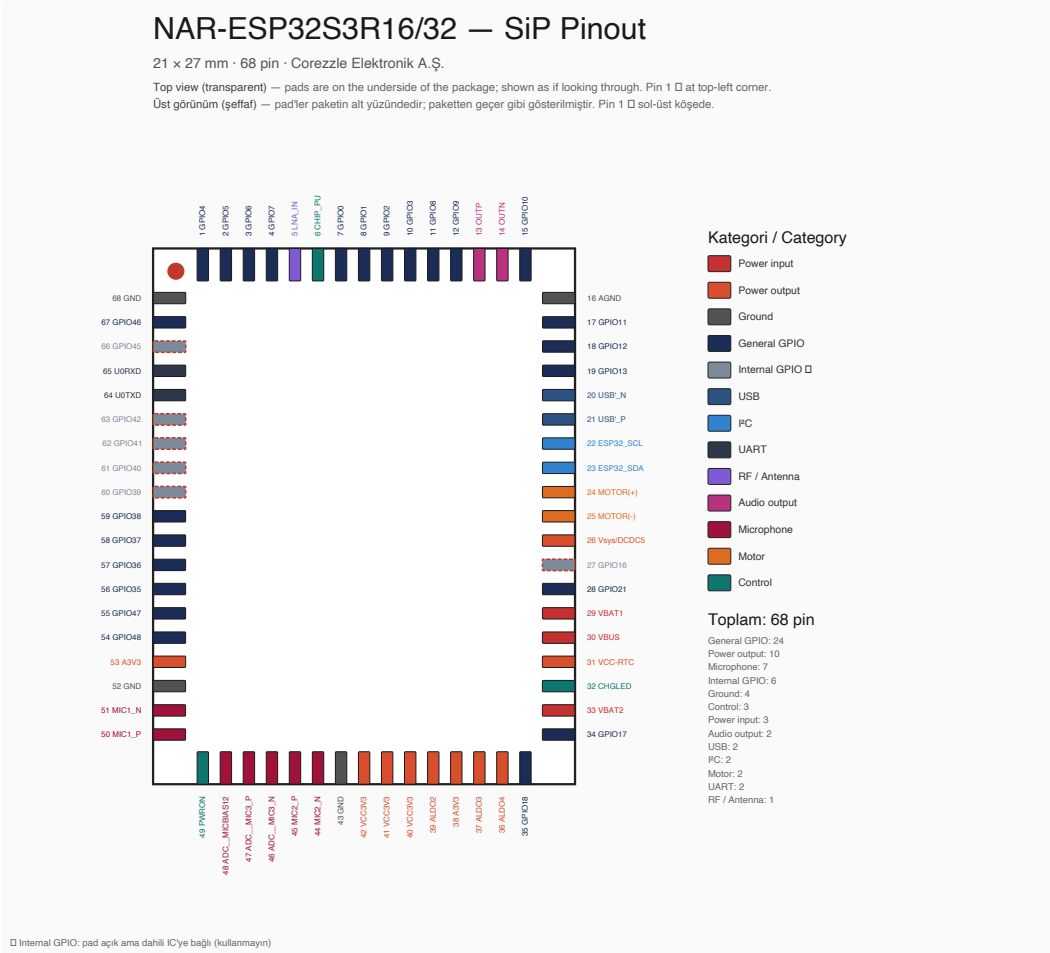

Figure 3.1. NAR-ESP32S3R16/32 68-pin LGA pinout (top view, transparent). Pin 1 marked with a red indicator in the top-left corner. Colors indicate pin category (power, GPIO, USB, I^2C, UART, RF, audio, microphone, motor, control).

3.2 Pin Function Table

Table 3.1 lists the primary function, type and on-package/off-package routing of each pin. For the complete alternate-function matrix, see the ESP32-S3 datasheet (chapter 14).

Table 3.1. NAR-ESP32S3R16/32 68-pin function table

Pin	Name	Type	Function / Connection
1	GPIO4	GPIO	ADC1_CH3, Touch4
2	GPIO5	GPIO	ADC1_CH4, Touch5
3	GPIO6	GPIO	ADC1_CH5, Touch6
4	GPIO7	GPIO	ADC1_CH6, Touch7
5	LNA_IN	RF	2.4 GHz antenna input (PCB or u.FL)
6	CHIP_PU	Control	System enable / reset (tied to AXP2101 PWRON)
7	GPIO0	GPIO	Boot strap — LOW ⇒ download mode
8	GPIO1	GPIO	ADC1_CH0, Touch1
9	GPIO2	GPIO	ADC1_CH1, Touch2
10	GPIO3	GPIO	ADC1_CH2, Touch3
11	GPIO8	GPIO	ADC1_CH7, Touch8
12	GPIO9	GPIO	ADC1_CH8, Touch9
13	OUTP	Audio out	ES8311 speaker/HP output (+)
14	OUTN	Audio out	ES8311 speaker/HP output (−)
15	GPIO10	GPIO	ADC1_CH9, Touch10
16	AGND	Ground	Analog ground (audio chain)
17	GPIO11	GPIO	ADC2_CH0, Touch11
18	GPIO12	GPIO	ADC2_CH1, Touch12
19	GPIO13	GPIO	ADC2_CH2, Touch13
20	USB_DN	USB	USB 2.0 D− (USBLC6-2SC6 ESD-protected)
21	USB_DP	USB	USB 2.0 D+ (USBLC6-2SC6 ESD-protected)
22	SCL	I^2C	System I^2C clock (PMIC + codec + mic ADC + RTC + IMU)
23	SDA	I^2C	System I^2C data (shared)
24	MOTOR+	Actuator	Vibration motor anode (MMBT3904 driver)
25	MOTOR−	Actuator	Vibration motor cathode (switched to GND)
26	Vsys/DCDC5	Power out	AXP2101 system rail / DCDC5
27	GPIO16[(1)]	GPIO	On-package I^2S BCK (shared ES8311 + ES7210)
28	GPIO21	GPIO	General-purpose or IMU/RTC/SD INT/CS
29	VBAT1	Power in	Li-Ion/LiPo battery input (AXP2101)
30	VBUS	Power in	USB-C 5 V input (AXP2101)
31	VCC-RTC	Power out	RTC backup supply (PCF85063)
32	CHGLED	Control	AXP2101 charge LED output
33	VBAT2	Power in	Battery input 2 (AXP2101 parallel)
34	GPIO17	GPIO	ADC2_CH6, Touch14
35	GPIO18	GPIO	General-purpose or IMU/RTC/SD INT/CS
36	ALDO4	Power out	AXP2101 ALDO4 (configurable)
37	ALDO3	Power out	AXP2101 ALDO3 (analog — IMU/RTC)
38	A3V3	Power out	Analog 3.3 V (ES8311 + ES7210)
39	ALDO2	Power out	AXP2101 ALDO2 (analog)
40	VCC3V3	Power out	System 3.3 V digital (DCDC1)
41	VCC3V3	Power out	System 3.3 V digital (DCDC1)
42	VCC3V3	Power out	System 3.3 V digital (DCDC1)
43	GND	Ground	System ground
44	MIC2_N	Microphone	ES7210 MIC2 channel (−, differential)

continued on next page

(continued)

Pin	Name	Type	Function / Connection
45	MIC2_P	Microphone	ES7210 MIC2 channel (+, differential)
46	MIC3_N	Microphone	ES7210 MIC3 channel (−)
47	MIC3_P	Microphone	ES7210 MIC3 channel (+)
48	MICBIAS12	Bias	ES7210 microphone bias (MIC1/MIC2)
49	PWRON	Control	AXP2101 power-on button input
50	MIC1_P	Microphone	ES7210 MIC1 channel (+)
51	MIC1_N	Microphone	ES7210 MIC1 channel (−)
52	GND	Ground	System ground
53	A3V3	Power out	Analog 3.3 V (second pad)
54	GPIO48	GPIO	High-speed digital
55	GPIO47	GPIO	High-speed digital
56	GPIO35	GPIO	High-speed digital
57	GPIO36	GPIO	High-speed digital
58	GPIO37	GPIO	High-speed digital
59	GPIO38	GPIO	High-speed digital
60	GPIO39[(1)]	GPIO	On-package — ICM-42670 INT1
61	GPIO40[(1)]	GPIO	On-package — ES8311 I^2S aux
62	GPIO41[(1)]	GPIO	On-package — I^2S WS/LRCK (shared ES8311 + ES7210)
63	GPIO42[(1)]	GPIO	On-package — ES7210 control
64	U0TXD	UART	ESP32-S3 U0TXD (GPIO43) — boot log + programming
65	U0RXD	UART	ESP32-S3 U0RXD (GPIO44) — programming
66	GPIO45[(1)]	GPIO	On-package — I^2S DATA (shared TDM)
67	GPIO46	GPIO	Boot strap, general purpose
68	GND	Ground	System ground

Note (1): *On-package use.* Although these pins are brought out as external pads, they are consumed by on-package chips. Driving or loading from outside is not recommended; they are exposed for test/debug only.

3.3 Pin Category Summary

Table 3.2 groups pins by functional category, providing a quick reference for the system designer.

3.4 ESP32-S3 GPIO ↔ SiP Pin Matrix

Table 3.3 shows where each ESP32-S3 GPIO maps onto the SiP pin and whether it is bound to an on-package chip. Critical reference for the software developer.

3.5 Unconnected / Invisible GPIOs

Although the ESP32-S3 has 45 GPIOs in total, several are not visible on the NAR-ESP32S3R16/32 external pin count:

- **GPIO14, GPIO15:** On-package only — used for I^2S MCLK and aux signals with the ES8311 codec. Not brought out.

Table 3.2. Pin category summary.

Category	Pins	Count
General-purpose GPIO	1–4, 7–12, 15, 17–19, 28, 34, 35, 54–59, 67	22
On-package GPIO[(1)]	27, 60–63, 66	6
USB 2.0	20, 21	2
System I^2C	22, 23	2
UART (boot)	64, 65	2
RF / antenna	5	1
Control (reset/IRQ/LED)	6, 32, 49	3
Audio output (codec)	13, 14	2
Microphone input (ADC)	44–48, 50, 51	7
Motor drive	24, 25	2
Power outputs (rails)	26, 31, 36–42, 53	11
Power inputs	29, 30, 33	3
Ground	16, 43, 52, 68	4
	Total	**68**

- **GPIO22–GPIO34:** These numbers do not exist on the ESP32-S3 (reserved by PSRAM).
- **GPIO19, GPIO20:** Routed as USB-C D−/D+; not accessible as separate digital GPIOs.

Table 3.3. ESP32-S3 GPIO — SiP pin mapping.

GPIO	SiP Pin	Dir	Bound chip	Function
0	7	I/O	—	Boot strap, ADC1_CH0
1	8	I/O	—	ADC1_CH0, Touch1
2	9	I/O	—	ADC1_CH1, Touch2
3	10	I/O	—	ADC1_CH2, Touch3
4	1	I/O	—	ADC1_CH3, Touch4
5	2	I/O	—	ADC1_CH4, Touch5
6	3	I/O	—	ADC1_CH5, Touch6
7	4	I/O	—	ADC1_CH6, Touch7
8	11	I/O	—	ADC1_CH7, Touch8
9	12	I/O	—	ADC1_CH8, Touch9
10	15	I/O	—	ADC1_CH9, Touch10
11	17	I/O	—	ADC2_CH0, Touch11
12	18	I/O	—	ADC2_CH1, Touch12
13	19	I/O	—	ADC2_CH2, Touch13
14	—	OUT	ES8311	I^2S MCLK (no external pad)
15	—	I/O	ES8311	I^2S aux (no external pad)
16	27	OUT	ES8311+ES7210	Shared I^2S BCK[(1)]
17	34	I/O	—	ADC2_CH6, Touch14
18	35	I/O	IMU/RTC/SD	On-package INT/CS
19	20	I/O	USB-C	USB D−
20	21	I/O	USB-C	USB D+
21	28	I/O	IMU/RTC/SD	On-package INT/CS
22–34	—	—	—	Not available (reserved by PSRAM)
35	56	I/O	—	High-speed digital
36	57	I/O	—	High-speed digital
37	58	I/O	—	High-speed digital
38	59	I/O	—	High-speed digital
39	60	I/O	IMU/RTC	On-package INT1[(1)]
40	61	I/O	ES8311	I^2S aux[(1)]
41	62	I/O	ES8311+ES7210	I^2S WS/LRCK[(1)]
42	63	I/O	ES7210	Mic ADC control[(1)]
43	64	OUT	UART0	TXD0
44	65	IN	UART0	RXD0
45	66	I/O	ES8311+ES7210	I^2S DATA TDM[(1)]
46	67	I/O	—	Boot strap, general
47	55	I/O	—	High-speed digital
48	54	I/O	—	High-speed digital

CHAPTER 4

Electrical Characteristics

4.1 Absolute Maximum Ratings

Warning: Exceeding these values may cause permanent damage to the device. These ratings represent stress limits only; functional operation of the device at these levels is **not guaranteed**. For operating conditions, see section 4.2.

The following values are based on the most *conservative* (tightest) limit from the on-package chip datasheets. For wider limits, consult the relevant upstream datasheet.

Table 4.1. Absolute maximum ratings (at package pins, referenced to GND).

Symbol	Parameter	Min	Max	Unit
V_{VBUS}	USB VBUS input (AXP2101)	−0.3	+6.0	V
V_{BAT}	Battery input VBAT1/2 (AXP2101)	−0.3	+4.5	V
V_{DD33}	3.3 V system rail (VCC3V3)	−0.3	+3.6	V
V_{IO}	GPIO drive voltage	−0.3	$V_{\mathrm{DD}} + 0.3$	V
$I_{\mathrm{IO,pin}}$	GPIO continuous current (per pin)	—	±40	mA
$I_{\mathrm{IO,tot}}$	GPIO total current (all pins)	—	±100	mA
T_{a}	Operating ambient temperature	−40	+85	°C
T_{stg}	Storage temperature	−65	+150	°C
T_{j}	Junction temperature	—	+125	°C
T_{sol}	Solder peak temperature (J-STD-020)	—	+260	°C
ΔT_{sol}	Solder peak duration (20–40 s)	—	40	s
$V_{\mathrm{ESD,HBM}}$	ESD Human Body Model (JS-001)	—	±2	kV
$V_{\mathrm{ESD,CDM}}$	ESD Charged Device Model (JS-002)	—	±500	V

The USB lines (D+, D–) withstand IEC 61000-4-2 level 4 ESD (±15 kV contact, ±25 kV air) thanks to the USBLC6-2SC6 TVS array.

4.2 Recommended Operating Conditions

4.3 DC Characteristics

DC characteristics apply at the ESP32-S3 external package pins ($V_{\mathrm{DD33}} = 3.3$ V, $T_{\mathrm{a}} = +25$ °C, unless otherwise noted).

Upstream Datasheet — ESP32-S3R16V

For full DC, AC and electrical parameters (timing diagrams, drive strength options, slew rate control), refer to Chapter 4 (Electrical Characteristics) of the Espressif ESP32-S3 datasheet:

`https://www.espressif.com/sites/default/files/documentation/esp32-s3_datasheet_en.pdf`

Table 4.2. Recommended operating conditions.

Symbol	Parameter	Min	Typ	Max	Unit
V_{VBUS}	USB VBUS	4.40	5.00	5.50	V
V_{BAT}	Li-Ion cell	3.00	3.70	4.20	V
V_{DD33}	3.3 V system rail (DCDC1)	3.20	3.30	3.40	V
V_{A33}	3.3 V analog rail (ALDO2/3)	3.20	3.30	3.40	V
V_{BLDO}	1.8 V backup rail (BLDO1)	1.71	1.80	1.89	V
T_a	Operating ambient temperature	−40	+25	+85	°C
$T_{a,RF}$	Operating temperature (RF performance)	−20	+25	+70	°C
f_{CPU}	ESP32-S3 CPU clock	80	240	240	MHz
f_{flash}	QSPI flash clock (DTR)	—	80	120	MHz

Table 4.3. GPIO DC characteristics.

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	Input high-level threshold	$0.75\,V_{DD}$	—	—	V
V_{IL}	Input low-level threshold	—	—	$0.25\,V_{DD}$	V
V_{OH}	Output high-level voltage	$0.8\,V_{DD}$	—	—	V
V_{OL}	Output low-level voltage	—	—	$0.1\,V_{DD}$	V
I_{OH}	Output source current (high-drive)	—	20	40	mA
I_{OL}	Output sink current (high-drive)	—	28	40	mA
I_{IL}	Input leakage current	—	—	±50	nA
R_{PU}	Internal pull-up resistance	—	45	—	kΩ
R_{PD}	Internal pull-down resistance	—	45	—	kΩ
C_{IN}	Input capacitance	—	2	—	pF

4.4 Power Consumption

The following values will be measured at $V_{BAT} = 3.7\,V$, $T_a = +25\,°C$, DCDC1 = 3.3 V. Table 4.4 reserves the configuration cells for bench characterization.

TBD (All power figures will be updated following bench characterization.)

4.5 Reset and Power-Up Sequencing

4.5.1 Power-Up Sequence

The system power-up sequence is automatically managed by the AXP2101 PMIC. Typical flow:

1. **Power source detection:** the AXP2101 detects the presence of VBUS (5 V) or VBAT (Li-Ion).
2. **Fault checks:** OVP, OTP, OCP protection checks.
3. **Soft-start:** DCDC1 (3.3 V) ramp-up (typ. **TBD** ms).
4. **Sequenced rail enable:** ALDO1–4 and BLDO1–2 enabled in order.
5. **CHIP_PU release:** once all rails are stable, the ESP32-S3 CHIP_PU pin is released (LOW → HIGH).

Table 4.4. Typical power-consumption profiles (bench measurement pending).

Mode	Typ	Max	Unit
Wi-Fi TX (peak, +20 dBm, 11b)	**TBD**	**TBD**	mA
Wi-Fi TX (average, 11n MCS7)	**TBD**	**TBD**	mA
Wi-Fi RX	**TBD**	**TBD**	mA
BLE TX (peak, +9 dBm, 1 Mbps)	**TBD**	**TBD**	mA
BLE 5 advertising (1 s interval)	**TBD**	**TBD**	µA
Modem-sleep (CPU 240 MHz, RF off)	**TBD**	**TBD**	mA
Modem-sleep (CPU 80 MHz, RF off)	**TBD**	**TBD**	mA
Light-sleep	**TBD**	**TBD**	µA
Deep-sleep (RTC + ULP)	**TBD**	**TBD**	µA
Hibernation (RTC + PMIC only)	**TBD**	**TBD**	µA

6. **ESP32-S3 boot:** ROM bootloader → second-stage bootloader → application.

TBD (Detailed power-up timing diagram (rail ramp times, EN deassert delay, boot time) will be added after bench measurement.)

4.5.2 Manual Reset

CHIP_PU (Pin 6) is the system reset line. Pulling this pin LOW for ≥ 1 ms resets the ESP32-S3. The PWRON (Pin 49) button on the AXP2101 triggers a system power-off through a long press (4 s by default).

4.5.3 Brown-Out Detection

The ESP32-S3 has an internal brown-out detector monitoring V_{DD33}; the system is reset if it drops below the programmable threshold. Default threshold 2.43 V, programmable range 2.13–2.82 V.

CHAPTER 5

RF Characteristics

The 2.4 GHz radio integrated within NAR-ESP32S3R16/32 operates through the ESP32-S3's internal PA/LNA block. The following values apply at $V_{BAT} = 3.7\,V$, $T_a = +25\,°C$ and $50\,\Omega$ load. Nominal values below are listed for reference; final values will be updated following anechoic-chamber measurement.

5.1 Wi-Fi (IEEE 802.11 b/g/n)

5.1.1 General Specifications

Table 5.1. Wi-Fi 2.4 GHz general specifications.

Feature	Value
Standard	IEEE 802.11 b/g/n
Frequency band	2.412 – 2.484 GHz (channels 1–14, region dependent)
Channel spacing	5 MHz (channels 1–13), 12 MHz (channel 14)
Modulation	DSSS (11b), OFDM (11g/n), CCK
HT mode	20 MHz, short/long GI
Max. data rate	72.2 Mbps (802.11n MCS7, 20 MHz, short GI)
Encryption	WPA / WPA2 / WPA3 / WEP
Modes	STA, AP, STA+AP, Mesh, Promiscuous

5.1.2 TX Output Power (Manufacturer nominal values)

Table 5.2. Wi-Fi TX output power (ESP32-S3 nominal, on-package PA, to be measured at antenna input).

Mode	Data rate	Nominal (dBm)	Tolerance (dB)
802.11b	1 Mbps DSSS	+21.0	±1.5
802.11b	11 Mbps DSSS	+20.5	±1.5
802.11g	6 Mbps OFDM	+20.0	±1.5
802.11g	54 Mbps OFDM	+18.0	±1.5
802.11n HT20	MCS0	+19.5	±1.5
802.11n HT20	MCS7	+16.0	±1.5

TBD (Final values will be updated following anechoic chamber measurement.)

Table 5.3. Wi-Fi receiver sensitivity (ESP32-S3 nominal).

Mode	Data rate / PER	Sensitivity (dBm)
802.11b	1 Mbps, PER $\leq$ 8%	−97.0
802.11b	11 Mbps, PER $\leq$ 8%	−89.0
802.11g	6 Mbps, PER $\leq$ 10%	−93.0
802.11g	54 Mbps, PER $\leq$ 10%	−75.0
802.11n HT20	MCS0, PER $\leq$ 10%	−92.0
802.11n HT20	MCS7, PER $\leq$ 10%	−72.5

5.1.3 RX Sensitivity

5.2 Bluetooth 5 LE + Mesh

5.2.1 General Specifications

Table 5.4. Bluetooth 5 LE general specifications.

Feature	Value
Version	Bluetooth 5.0 LE
PHY support	1 Mbps, 2 Mbps, Coded (S=2, S=8)
Roles	Master, Slave, Broadcaster, Observer, concurrent
Topology	Point-to-point, Mesh, Star
Max. payload (LE 2M)	251 bytes
Adv. packet size	31 / 255 bytes (legacy / extended)
Frequency hops	40 channels, 2 MHz spacing

5.2.2 TX Output Power

Table 5.5. BLE TX output power (ESP32-S3 nominal).

PHY	Configuration	Nominal (dBm)	Tolerance (dB)
1 Mbps	High power	+18.0	±1.5
1 Mbps	Normal	+9.0	±1.5
2 Mbps	High power	+18.0	±1.5
Coded (S=2)	Long-range	+17.5	±1.5
Coded (S=8)	Long-range	+17.0	±1.5

5.2.3 RX Sensitivity

TBD (Final values will be updated following anechoic chamber measurement.)

Table 5.6. BLE receiver sensitivity (ESP32-S3 nominal).

PHY	Condition	Sensitivity (dBm)
1 Mbps	BER $\leq 10^{-3}$, dirty TX off	−97.0
2 Mbps	BER $\leq 10^{-3}$, dirty TX off	−94.0
Coded (S=2)	BER $\leq 10^{-3}$, FEC	−99.0
Coded (S=8)	BER $\leq 10^{-3}$, FEC	−103.0

5.3 Antenna Options

NAR-ESP32S3R16/32 supports two antenna configurations:

5.3.1 On-Package PCB Antenna

A PIFA-style antenna embedded in the package; no external component required. The antenna input (Pin 5, LNA_IN) is routed inside the package to the antenna structure. This mode is sufficient for the majority of development cycles.

- Type: PIFA (Planar Inverted-F)
- Polarization: Linear
- Antenna gain (peak): **TBD** dBi
- Impedance: 50 Ω

5.3.2 External u.FL / IPEX MHF1

Through pin configuration, the RF output can be routed outside the package (selected at manufacture; no field change). In this mode the developer adds their own antenna design; re-certification is required.

TBD (Antenna gain, radiation pattern and total radiation efficiency (η_{rad}) will be added following anechoic-chamber measurements.)

5.4 Regulatory Certification Status

Table 5.7. Regulatory certification targets (planned, pending).

Region	Certification	Status
EU	CE-RED (EN 300 328, EN 301 489-17)	**TBD** Q3 2026
USA	FCC Part 15.247 / Part 15B	**TBD** Q3 2026
Canada	ISED RSS-247	**TBD** Q3 2026
Japan	MIC (Giteki)	**TBD** Q4 2026
Bluetooth SIG	Declaration ID (BLE 5)	**TBD** Q3 2026
Wi-Fi Alliance	Wi-Fi CERTIFIED	**TBD** Q4 2026

TBD (Certification numbers (FCC ID, IC ID, MIC number, Bluetooth Declaration ID, CE notified body reference) will be added once the approval process is complete.)

Upstream Datasheet — ESP32-S3 RF

For full Wi-Fi and BLE radio specifications, RF calibration procedure, PHY parameter tables and regulatory test reference values, refer to Chapters 3 (Wi-Fi) and 4 (Bluetooth) of the Espressif ESP32-S3 datasheet:
`https://www.espressif.com/sites/default/files/documentation/esp32-s3_datasheet_en.pdf`

CHAPTER 6

On-Package Peripherals

This chapter details the SiP-specific connectivity and configuration of the peripheral chips integrated within the package. The complete electrical datasheet for each chip is referenced via the manufacturer's official sources (see chapter 14).

6.1 Audio Codec — ES8311

The ES8311 is a mono I^2S codec with a built-in 32 Ω speaker/HP driver. It is connected to the I^2S_0 peripheral of the ESP32-S3.

6.1.1 SiP Integration

Table 6.1. ES8311 SiP integration details.

Parameter	Value / Connection
ESP32-S3 interface	$I^2S_0 + I^2C_0$
I^2C address	`0x18` (7-bit, `0x30`/`0x31` 8-bit)
MCLK (GPIO14, on-package)	12.288 MHz or bit clock × 256
BCK (GPIO16, on-package shared)	sample rate × 64 (TDM)
WS/LRCK (GPIO41, on-package shared)	sample rate (typ. 16/48/96 kHz)
DATA (GPIO45, on-package shared TDM)	—
Output pins (off-package)	OUTP (Pin 13), OUTN (Pin 14)
Analog supply	ALDO2 (3.3 V, max 300 mA)
Digital supply	DCDC1 (3.3 V)

6.1.2 Performance Summary (Manufacturer nominal)

Upstream Datasheet — ES8311

For full THD+N, SNR, register map and DAC/HP/ADC characteristics, refer to the Everest Semi ES8311 datasheet:
`https://www.everest-semi.com/pdf/ES8311DS.pdf`

6.2 Microphone ADC — ES7210

The ES7210 is a 4-channel digital microphone ADC connected to the ESP32-S3 over TDM. Aimed at voice IoT and sound-source-localization (SSL) applications.

Table 6.2. ES8311 performance summary (manufacturer datasheet).

Parameter	Condition	Nominal
DAC SNR (A-weighted)	1 kHz, 0 dBFS, FS=48 kHz	110 dB
DAC THD+N	1 kHz, −3 dBFS	−92 dB
ADC SNR (A-weighted)	1 kHz, mic input	100 dB
ADC THD+N	1 kHz, −3 dBFS	−86 dB
HP driver output power	16 Ω, THD ≤ 1%	35 mW
HP driver output power	32 Ω, THD ≤ 1%	25 mW
Sample rate range	I^2S	8 – 96 kHz
Bit depth	I^2S	16, 18, 20, 24, 32 bit
Frequency response	±0.1 dB	20 Hz – 20 kHz

Table 6.3. ES7210 SiP integration details.

Parameter	Value / Connection
ESP32-S3 interface	TDM (GPIO39–42, 45 shared) + I^2C_0
I^2C address	`0x40` (7-bit, `0x80`/`0x81` 8-bit)
Channel count	4 (differential or single-ended microphones)
Microphone pins (off-package)	MIC1/2/3 (Pin 44–47, 50, 51) + bias (Pin 48)
Bias voltage	0.9 – V_{A33}, programmable
Analog supply	ALDO3 (3.3 V, max 300 mA)
Digital supply	DCDC1 (3.3 V)

6.2.1 SiP Integration

6.2.2 Performance Summary (Manufacturer nominal)

Table 6.4. ES7210 performance summary (manufacturer datasheet).

Parameter	Condition	Nominal
SNR (A-weighted)	1 kHz, FS=48 kHz, PGA=0 dB	105 dB
THD+N	1 kHz, −3 dBFS	−90 dB
Resolution	Per channel	24-bit
Sample rate range	TDM	8 – 96 kHz
Channel isolation	—	≥ 90 dB
PGA gain range	Programmable, 3 dB steps	0 – 36 dB
DC blocking filter	First-order HPF, programmable	0 – 100 Hz

Upstream Datasheet — ES7210

For full TDM, SNR, channel isolation and register map details, refer to the Everest Semi ES7210 datasheet:
`https://www.everest-semi.com/pdf/ES7210DS.pdf`

6.3 IMU — ICM-42670-P

The ICM-42670-P is a 6-axis (gyro + accel) inertial measurement unit with a built-in 2.25 KB FIFO and the APEX motion engine.

6.3.1 SiP Integration

Table 6.5. ICM-42670-P SiP integration details.

Parameter	Value / Connection
ESP32-S3 interface	I^2C_0 (default) or SPI (10 MHz max)
I^2C address	`0x68` (AD0=0)
INT1 (GPIO39, on-package)	DRDY, FIFO watermark, motion event, APEX
Supply	DCDC1 (3.3 V)
Sleep current	3.5 µA typ.

6.3.2 Performance Summary (Manufacturer nominal)

Table 6.6. ICM-42670-P performance summary (manufacturer datasheet, $T_a = +25$ °C).

Parameter	Condition	Nominal
Gyro full-scale ranges	—	±250 / ±500 / ±1000 / ±2000 dps
Accel full-scale ranges	—	±2 / ±4 / ±8 / ±16 g
Gyro noise density	low-noise mode	0.007 dps/$\sqrt{\text{Hz}}$
Accel noise density	low-noise mode	**TBD**
Gyro / accel offset drift	−40 °C – +85 °C	**TBD**
ODR range	—	**TBD**
Operating current (6-axis)	low-noise mode	0.55 mA
Accel low-power current	ODR=1.56 Hz	4.4 µA
Sleep current	—	3.5 µA
Host interface	—	I^2C 1 MHz, I3C 12.5 MHz, SPI 24 MHz

Upstream Datasheet — ICM-42670-P

For full gyro/accel accuracy, noise PSD, ODR settings and FIFO configuration, refer to the TDK InvenSense ICM-42670-P datasheet:
`https://invensense.tdk.com/en-us/products/6-axis/icm-42670-p`

6.4 RTC — PCF85063ATL

The PCF85063ATL is an I^2C RTC with an integrated 32.768 kHz quartz oscillator. Its low-power alarm function allows waking the ESP32-S3 from deep-sleep.

Table 6.7. PCF85063ATL SiP integration details.

Parameter	Value / Connection
ESP32-S3 interface	I^2C_0
I^2C address	`0x51` (7-bit)
INT (on-package, shared with GPIO39)	Alarm, periodic timer
Backup supply (off-package, Pin 31)	VCC-RTC (programmable 1.8–3.6 V)
Core supply	BLDO1 (1.8 V battery-backup)

6.4.1 SiP Integration

6.4.2 Performance Summary (Manufacturer nominal)

Table 6.8. PCF85063ATL performance summary.

Parameter	Condition	Nominal
Crystal frequency	—	32.768 kHz
Clock accuracy	+25 °C	±20 ppm
Temperature curve	−10 °C – +50 °C	parabolic, peak +25 °C
Core current (oscillator)	$V_{DD} = 1.8$ V	200 nA typ.
Core current (oscillator)	$V_{DD} = 3.3$ V	700 nA typ.
I^2C max. speed	Fast mode plus	1 MHz
Data retention	—	lifetime

Upstream Datasheet — PCF85063ATL

For the full date/time register set, alarm configuration, temperature accuracy curve and I^2C protocol, refer to the NXP PCF85063A datasheet:
`https://www.nxp.com/docs/en/data-sheet/PCF85063A.pdf`

6.5 Flash Memory — GD25LQ256DWIGR

The GD25LQ256 is a 32 MB (256 Mbit) QSPI NOR flash, connected to the ESP32-S3 integrated flash interface and timing-calibrated at the factory. Used to store the boot ROM, application, NVS (non-volatile storage) and the filesystem.

6.5.1 SiP Integration

6.5.2 Performance Summary

Upstream Datasheet — GD25LQ256

For full read/write timing, QSPI mode configuration, advanced security features and the command set, refer to the GigaDevice GD25LQ256 datasheet:
`https://www.gigadevice.com/datasheet/gd25lq256e/`

Table 6.9. GD25LQ256 SiP integration details.

Parameter	Value / Connection
Capacity	256 Mbit (32 MB)
Interface	QSPI (1-1-4 / 1-4-4 / 4-4-4 DTR)
Voltage range	1.65 – 1.95 V or 2.7 – 3.6 V
ESP32-S3 connection	On-package QSPI line (Vssp internal rail)
Supply	DCDC1 (3.3 V)

Table 6.10. GD25LQ256 performance summary.

Parameter	Condition	Nominal
Max. read rate	STR (single transfer)	133 MHz
Max. read rate	DTR (double transfer)	80 MHz (160 Mbps eq.)
Page size	—	256 B
Sector size	—	4 kB
Block size	—	32 / 64 kB
Page program time	256 B	0.45 ms typ.
Sector erase time	4 kB	90 ms typ.
Chip erase time	32 MB	240 s typ.
Endurance	write cycles/sector	100,000
Data retention	+55 °C	20 years

6.6 USB-C ESD Protection — USBLC6-2SC6

The USBLC6-2SC6 is a two-line TVS array for USB 2.0 D+/D– lines, providing IEC 61000-4-2 level 4 ESD protection.

Table 6.11. USBLC6-2SC6 protection characteristics.

Parameter	Condition	Nominal
Operating voltage range (rev.)	—	0 – 5.25 V
Reverse breakdown voltage	$I_R = 1$ mA	6.0 V min
ESD strike (contact)	IEC 61000-4-2 level 4	±15 kV
ESD strike (air)	IEC 61000-4-2 level 4	±25 kV
Clamping voltage	$I_{PP} = 1$ A	17 V typ.
Dynamic resistance	TLP, 8/20 µs	0.1 Ω
D+/D– capacitance (to GND)	$V_{BIAS} = 0$ V	3.5 pF typ.

Upstream Datasheet — USBLC6-2SC6

For full ESD-energy absorption curves, IEC 61000-4-2 classification and clamp-voltage graphs, refer to the STMicroelectronics USBLC6-2SC6 datasheet:
`https://www.st.com/resource/en/datasheet/usblc6-2.pdf`

CHAPTER 7

Power Management and Distribution

7.1 AXP2101 PMIC — Overview

The X-Powers AXP2101 is the central power-management chip of NAR-ESP32S3R16/32. The following blocks are integrated in a single package:

- Single-cell Li-Ion/LiPo linear charge controller (from a 5 V/USB VBUS input)
- 5 × buck DC-DC converters (DCDC1–5)
- 4 × linear LDOs (ALDO1–4) for the main system rails
- 2 × battery-backup LDOs (BLDO1–2) for low-power retention rails
- I^2C register interface, OTP configuration
- 12-bit ADC: VBAT, VBUS, TS, die temperature, IBAT
- Power button, IRQ, protective safety (OVP, OCP, OTP, UVP)
- Power-path: the system is fed from VBUS when present and the battery does not discharge

7.2 Input Specifications

Table 7.1. AXP2101 input specifications.

Parameter	Condition	Min	Typ	Max
V_{VBUS}	USB VBUS voltage	3.9	5.0	5.5
I_{VBUS}	VBUS input current (programmable limit)	—	500 mA	2 A
V_{BAT}	Li-Ion cell voltage	2.5	3.7	4.5
V_{UVLO}	Under-voltage lockout	—	2.5	—
T_{op}	Operating temperature	−40	—	+85 (°C)

7.3 Rail Specifications

Table 7.2 lists the voltage range, current capability and actual on-package use of every rail the AXP2101 provides. The “Pin” column indicates whether the rail is brought outside the NAR-ESP32S3R16/32 package.

Table 7.2. AXP2101 rail mapping — actual use within the SiP.

Rail	Voltage	Current	Efficiency	Load (on-package)	Pin
DCDC1	1.5 – 3.4 V → 3.3 V	2.0 A	> 90 %	ESP32-S3, flash, IMU, RTC, codec digital	—
DCDC2	0.5 – 1.54 V programmable	1.5 A	> 88 %	— (user configuration)	**TBD**
DCDC3	0.5 – 3.4 V programmable	1.5 A	> 88 %	— (user configuration)	**TBD**
DCDC4	0.5 – 3.4 V programmable	1.5 A	> 88 %	— (user configuration)	**TBD**
DCDC5	1.2 – 3.7 V programmable	1.5 A	> 86 %	Vsys output	26
ALDO1	0.5 – 3.5 V → 1.8 V	300 mA	—	RF, PLL analog	—
ALDO2	0.5 – 3.5 V → 3.3 V	300 mA	—	ES8311 analog	39
ALDO3	0.5 – 3.5 V → 3.3 V	300 mA	—	ES7210 analog, IMU	37
ALDO4	0.5 – 3.5 V programmable	300 mA	—	— (user)	36
BLDO1	0.5 – 3.5 V → 1.8 V	150 mA	—	PCF85063 RTC (battery-backup)	—
BLDO2	0.5 – 3.5 V programmable	150 mA	—	— (user)	**TBD**

Table 7.3. DCDC rail performance (typical).

Parameter	Condition	Nominal
Output voltage accuracy	PWM mode	±2%
Output ripple	PWM, full load, 1.2 MHz	30 mV pp typ.
Transient response	100 mA → 1 A	< 100 µs
Output current limit	Programmable	0.5 – 2.0 A
Soft-start time	Default	1 ms

7.3.1 Rail Performance

7.4 Charge Control

The AXP2101 provides pre-charge, constant-current (CC), constant-voltage (CV) and thermal protection for single-cell Li-Ion/LiPo batteries.

7.5 Power-Path

Thanks to the AXP2101's built-in power-path logic:

- When VBUS is present and ≥ 4.4 V, the system is fed from VBUS and the battery *does not discharge*. Charging proceeds in parallel.
- When VBUS is absent, the system seamlessly switches to the battery (uninterrupted, < 10 µs).
- When VBUS provides insufficient current (load > VBUS limit), the deficit is supplied from the battery (boost mode).

7.6 ADC Channels

System monitoring channels readable via I^2C (12-bit resolution):

Table 7.4. Li-Ion charge parameters (AXP2101).

Parameter	Description / Range	Default
Charge current (CC)	0 – 1.0 A, 25 mA steps	500 mA
Termination voltage (CV)	4.10 / 4.20 / 4.35 / 4.40 V	4.20 V
Pre-charge current (trickle)	$V_{BAT} < 3.0$ V	100 mA
Pre-charge threshold	—	3.0 V
Thermal protection (TS)	NTC (β=3950, 10 kΩ@25°C)	optional
Thermal shutdown threshold	T_{die}	+135 °C
End-of-charge current	5 – 20% I_{CC}	10%
Charge timer	Programmable	10 hours

Table 7.5. AXP2101 ADC channels.

Channel	Measured quantity	Resolution
VBAT	Battery voltage	1 mV
VBUS	USB input voltage	1 mV
IBAT	Battery charge/discharge current	1 mA
TS	NTC temperature probe	0.5 mV
T_{die}	PMIC die temperature	0.1 °C

Upstream Datasheet — AXP2101

For full rail specifications, OTP configuration, register map and I^{2}C protocol, refer to the X-Powers AXP2101 datasheet:
`https://github.com/CinaryEmbedded/AXP2101-Datasheet`

7.7 Power-Up Sequencing

The system power-up sequence is automatically managed by the AXP2101 PMIC; OTP configuration defines the sequencing priority for every rail. Sequencing changes are made on the manufacturer side only.

TBD (Detailed power-up timing diagram (rail ramp times, EN deassert delay, boot time) will be added after bench measurement. Order: VBUS/VBAT detect → AXP2101 fault check → DCDC1 ramp ($\leq$ 1 ms) → ALDO/BLDO sequential enable → CHIP_PU release → ESP32-S3 flash boot.)

CHAPTER 8

Boot and Programming

8.1 Boot Flow

On power-up or reset, NAR-ESP32S3R16/32 follows a three-stage boot process:

1. **ROM bootloader:** the first-stage bootloader residing in the ESP32-S3 internal mask ROM. It samples the strapping pins and determines the operating mode (SPI Boot / Download Mode).
2. **Second-stage bootloader:** `bootloader.bin` residing in flash; it loads the partition table, selects which application image to load (OTA), and performs security checks (Secure Boot v2, Flash Encryption).
3. **Application:** the selected application image is either loaded into RAM or executed directly from flash in XIP mode.

8.2 Strap Pins

The ESP32-S3 boot mode is determined by the levels of the strap pins at reset. Strap pins accessible on NAR-ESP32S3R16/32 and their effects:

Table 8.1. Boot strap pins (latched at reset).

Strap pin	SiP pin	Function	Default / Behaviour
GPIO0	7	Boot mode select	Internal pull-up — HIGH ⇒ SPI Boot, LOW ⇒ Download
GPIO3	10	JTAG select (within ROM)	Float ⇒ USB-Serial-JTAG; HIGH ⇒ MTDI-MTMS JTAG
GPIO45	66	VDD_SPI select(1)	Low ⇒ flash 3.3 V (default, on-package GD25LQ256)
GPIO46	67	ROM message output control	LOW ⇒ ROM messages suppressed

(1) **Caution:** GPIO45 is used internally for the I^2S DATA line (see Table 3.3). Its strap function is set to the correct level at the factory; external manipulation is not recommended.

8.3 Download Mode (Programming)

8.3.1 Automatic Download

When connected over USB-C, `esptool.py` automatically triggers the following sequence:

1. Drives CHIP_PU (Pin 6) LOW → HIGH through DTR/RTS (reset)
2. Holds GPIO0 (Pin 7) LOW
3. ROM bootloader enters download mode
4. `esptool.py` starts the flash read/write protocol

8.3.2 Manual Download

For manual download mode:

1. Pull GPIO0 (Pin 7) to GND
2. Pulse CHIP_PU (Pin 6) LOW for 1 ms and release
3. Release GPIO0

8.4 USB-Serial-JTAG

The ESP32-S3's integrated USB-Serial-JTAG peripheral allows direct PC connectivity without an external USB-UART bridge. NAR-ESP32S3R16/32 brings the D+/D– lines to the USB-C connector through the on-package USBLC6-2SC6 protector.

Table 8.2. USB-Serial-JTAG characteristics.

Feature	Value
USB class	USB 2.0 Full-Speed (12 Mbps)
USB Vendor / Product ID	VID `0x303A` / PID `0x1001` (Espressif default)
Virtual serial port (CDC-ACM)	`esptool.py`, `idf.py monitor`, gdb
JTAG bridge	OpenOCD (adapter: `esp_usb_jtag`)
DFU	Device Firmware Update class (ESP-IDF option)
Endpoints	4 (CDC IN/OUT + JTAG IN/OUT)

USB-Serial-JTAG keeps working even when the system cannot boot, enabling flash recovery from a "bricked" state.

8.5 eFuse Configuration

The ESP32-S3 eFuse block holds one-time programmable (OTP) configuration and security parameters, written either at the manufacturer side or in the field.

Table 8.3. eFuse blocks — overview.

Block	Contents	Capacity
BLOCK0	System configuration (boot register, USB CDC control)	256-bit
BLOCK1	MAC address (Wi-Fi, BT, Eth, IPv6) + ADC calibration	256-bit
BLOCK2	System backup MAC + calibration	256-bit
BLOCK3 (USER_DATA)	User OTP	256-bit
BLOCK4-8 (KEY_DATA)	Secure Boot / Flash Encryption keys	5×256-bit
BLOCK9 (SYS_DATA)	Espressif system data	256-bit
BLOCK10 (SYS_DATA2)	Espressif system data 2	256-bit

Important: eFuse writes are irreversible. Every operation performed with `espefuse.py` in a production environment must be logged.

8.6 Security Features

8.6.1 Secure Boot v2

RSA-3072 signature-based secure boot. Once the key digest has been written into eFuse, only signed images can be booted.

8.6.2 Flash Encryption

AES-256-XTS encryption protects code and data stored in flash. The key is written to eFuse; decryption is performed in hardware and the plaintext is loaded into RAM, never written back to flash.

8.6.3 HMAC and Digital Signature Peripherals

Hardware-accelerated HMAC-SHA256 and RSA digital signature units for TLS handshake and device attestation.

8.7 Programming Flow

1. Connect the device to the PC via USB-C
2. Detect the device with `esptool.py --chip esp32s3 chip_id`
3. Flash with `idf.py build flash monitor` (ESP-IDF) or `arduino-cli upload` (Arduino)
4. The application starts automatically after reset

Upstream Datasheet — ESP32-S3 Boot

For boot strap pin behaviour, eFuse map, Secure Boot v2 and Flash Encryption details, refer to Chapter 2.1 (Boot Configuration) of the ESP32-S3 datasheet and to the ESP-IDF Get Started guide:
`https://docs.espressif.com/projects/esp-idf/en/latest/esp32s3/get-started/`

CHAPTER 9

Mechanical Information

9.1 Package Overview

NAR-ESP32S3R16/32 is housed in a square-cornered rectangular **LGA-68** (Land Grid Array, castellated) package. All 68 pads sit on the bottom face of the package, lined along the four edges; the castellated edges allow the package to be used both in a reflow SMT flow and in manual prototype soldering.

- Package type: LGA-68 (castellated edge)
- Pad layout: along four edges (19 left + 19 right + 15 top + 15 bottom) — portrait orientation
- Mounting: SMT (recommended) or manual soldering
- Visible marking: Pin 1 dot on the top face of the package (top-left corner)

9.2 Package Dimensions (Nominal)

The table below lists the nominal mechanical dimensions of the package. Tolerances follow JEDEC MO-220; will be updated in the final production revision after die measurements.

Table 9.1. Package nominal dimensions.

Symbol	Dimension	Description	Min	Nominal	Max
L	Long edge	Package outer length (vertical)	26.90	27.00	27.10
W	Short edge	Package outer width (horizontal)	20.90	21.00	21.10
H	Height (total)	Package outer height	1.80	1.90	2.00
h	Substrate thickness	Lower PCB-style base layer	0.55	0.60	0.65
p_{LR}	Pad pitch (left/right)	Pad pitch along long edge	1.27	1.278	1.29
p_{TB}	Pad pitch (top/bottom)	Pad pitch along short edge	1.20	1.214	1.22
d_{L}	Pad long dim.	Castellation depth	1.05	1.10	1.15
d_{W}	Pad short dim.	Pad width	0.55	0.60	0.65

All values are in millimetres (mm).

9.3 Pad Geometry

All pads share the same geometry (uniform LGA layout). Looking from the pad plane, each pad's short edge is perpendicular to the outer package edge, and its long edge is parallel to it.

- Pad size: $0.60 \times 1.10\,\mathrm{mm}$ (W $\times$ L)
- Pad count: 68 (uniform, 19 left + 19 right + 15 top + 15 bottom)
- Pad finish: ENIG (Electroless Nickel Immersion Gold), Au $\geq 0.05\,\mu\mathrm{m}$
- Castellation: the pad's outer edge is recessed into the package side wall

- Pin 1 marker: silkscreen dot, top-left corner

9.4 Mechanical Drawing

Figure 9.1 shows a 3D isometric view of the package. Figure 9.2 provides 2D top + side views with dimension labels. Figure 9.3 shows the top pinout view and pad numbering order. Pin 1 is marked in the top-left corner with a red indicator; pin numbering advances counter-clockwise.

9.5 Recommended Land Pattern (IPC-7351B)

For the SMT design of NAR-ESP32S3R16/32, the following IPC-7351B "Nominal" (Medium) land pattern is recommended.

Table 9.2. Recommended IPC-7351B land pattern parameters.

Parameter	Description	Recommended
Land length	Enters the castellation + outer overhang	1.30 mm
Land width	Pad width + 0.10 mm each side	0.80 mm
Land pitch (left/right)	Matches package pitch	1.278 mm
Land pitch (top/bottom)	Matches package pitch	1.214 mm
Solder paste coverage	80% of pad area (small stencil offset)	0.60 × 1.05 mm
Stencil thickness	—	0.127 mm (5 mil)
Pin 1 marker	PCB silkscreen, 0.5 mm outside the package	0.5 mm ∅

TBD (The complete land pattern drawing (PDF) will be published in the next revision.)

9.6 Tape & Reel Information

NAR-ESP32S3R16/32 ships in **tape & reel** (T&R) and **tray** formats. T&R is intended for high-volume SMT manufacturing; tray is intended for small-batch prototype and test runs.

Table 9.3. Tape & reel packaging parameters (planned).

Parameter	Description	Value
Carrier tape width (W)	EIA-481 compliant	32 mm
Pocket A0	Package length + tolerance	27.40 mm
Pocket B0	Package width + tolerance	21.40 mm
Pocket K0	Package height + tolerance	2.10 mm
Pocket pitch (P_1)	Between pocket centres	28.00 mm
Sprocket hole pitch (P_0)	—	4.00 mm
Reel diameter	13″ (330 mm) standard	—
Parts per reel	13″ reel	**TBD**
Reel weight (full)	—	**TBD** kg

9.7 Reflow Profile

The reflow profile recommended for NAR-ESP32S3R16/32 follows the parameter ranges of **IPC/JEDEC J-STD-020E** (*Moisture/Reflow Sensitivity Classification for Nonhermetic Surface Mount Devices*, Table 4-2). The package classifies as:

- **Package volume:** $21 \times 27 \times 1.9 = 1077\,\text{mm}^3 \Rightarrow$ J-STD-020E "Large body" class (height $> 1.6\,\text{mm}$)
- T_{peak} **ceiling for this class:** 260 °C (Table 4-2)
- **Solder alloy assumption:** SAC305 (Sn96.5/Ag3.0/Cu0.5), liquidus $T_L = 217\,°\text{C}$. If a different alloy is used, T_L changes and the profile must be adjusted
- **MSL class:** MSL3, multi-reflow tolerance 3 passes (see section 9.8)

Figure 9.4 shows the typical recommended temperature-time curve. **The actual bench profile will be added in the final revision following MSL3 characterization during production.**

Table 9.4. Recommended reflow profile — J-STD-020E Table 4-2 "Large body" class, SAC305 solder assumed.

Zone	Description	Target
Preheat ramp	Room $\rightarrow$ 150 °C, ≤ 3 °C/s	60 – 90 s
Soak (preheat zone)	150 – 200 °C	60 – 120 s
Reflow ramp (above liquidus)	200 °C $\rightarrow$ peak, ≤ 3 °C/s	60 – 90 s
Peak temperature (T_{peak})	MSL3 limits	245 – 260 °C
Peak time	Above $T_{\text{peak}} - 5$ °C	10 – 30 s
Time above liquidus (t_{L})	$T_{\text{L}} = 217$ °C (SAC305)	60 – 90 s
Cooling	Peak $\rightarrow$ 100 °C, ≤ 6 °C/s	—

9.7.1 Reflow Tolerance of On-Package Chips

The reflow tolerance of the NAR-ESP32S3R16/32 SiP is set by the on-package chip with the tightest tolerance. The following table compiles the typical tolerance of every active chip from its manufacturer datasheet.

Table 9.5. Reflow tolerance of on-package chips (typical, per manufacturer datasheets).

Chip	Manufacturer	MSL	$T_{\text{peak,max}}$
ESP32-S3R16V	Espressif	MSL3	260 °C
GD25LQ256DWIGR	GigaDevice	MSL3	260 °C
AXP2101	X-Powers	MSL3	260 °C
ES8311	Everest Semi	MSL3	260 °C
ES7210	Everest Semi	MSL3	260 °C
ICM-42670-P	TDK InvenSense	MSL3	260 °C
PCF85063ATL	NXP	MSL1	260 °C
USBLC6-2SC6	ST	MSL1	260 °C
SiP tolerance	**(weakest link)**	**MSL3**	**260 °C**

Therefore the recommended profile keeps $T_{\text{peak}} \leq 260$ °C; the target window is 245–260 °C with peak time ≤ 30 s. The profile remains within the J-STD-020E limits.

TBD (The MSL class of every chip will be re-confirmed against the manufacturer datasheet in the final production revision. The values in the table use the typical $T_{\text{peak,max}} = 260$ °C; some manufacturers may specify tighter limits.)

9.7.2 Solder Flux Selection

- ROL0 / ROL1 (rosin-based, no-clean): recommended
- REL0 (resin-based): acceptable
- ORL0 / ORM1 (organic, no-clean): should not be used in high-humidity environments (intra-package residue buildup)

9.8 Moisture Sensitivity Level (MSL)

NAR-ESP32S3R16/32 is J-STD-020 **MSL3** class.

- After removal from vacuum-sealed packaging, the device must be reflowed within **168 hours** (7 days) ($\leq$ 30 °C, $\leq$ 60% RH ambient).
- If this time is exceeded, the parts must be reset by baking (125 °C, 24 hours).
- Shelf life inside vacuum-sealed packaging: **12 months**.

TBD (The MSL class will be verified in the final production revision; MSL3 has been assessed on pre-production samples.)

9.9 ESD Handling

NAR-ESP32S3R16/32 is a sensitive semiconductor device. The following ESD precautions must be observed during handling:

- Grounded workstation, ESD wrist strap
- Conductive floor mat or static-dissipative surface
- An exposed device must not be kept outside an ESD-safe environment for $\geq$ 5 seconds
- Devices must not be exposed to open atmosphere outside ESD-safe packaging (pouch, tray, T&R)



Figure 9.1. NAR-ESP32S3R16/32 3D view — top-right: front face (silkscreen marking and regulator ID fields), bottom-left: back face (68 castellated pads, edge layout 15+15+19+19).

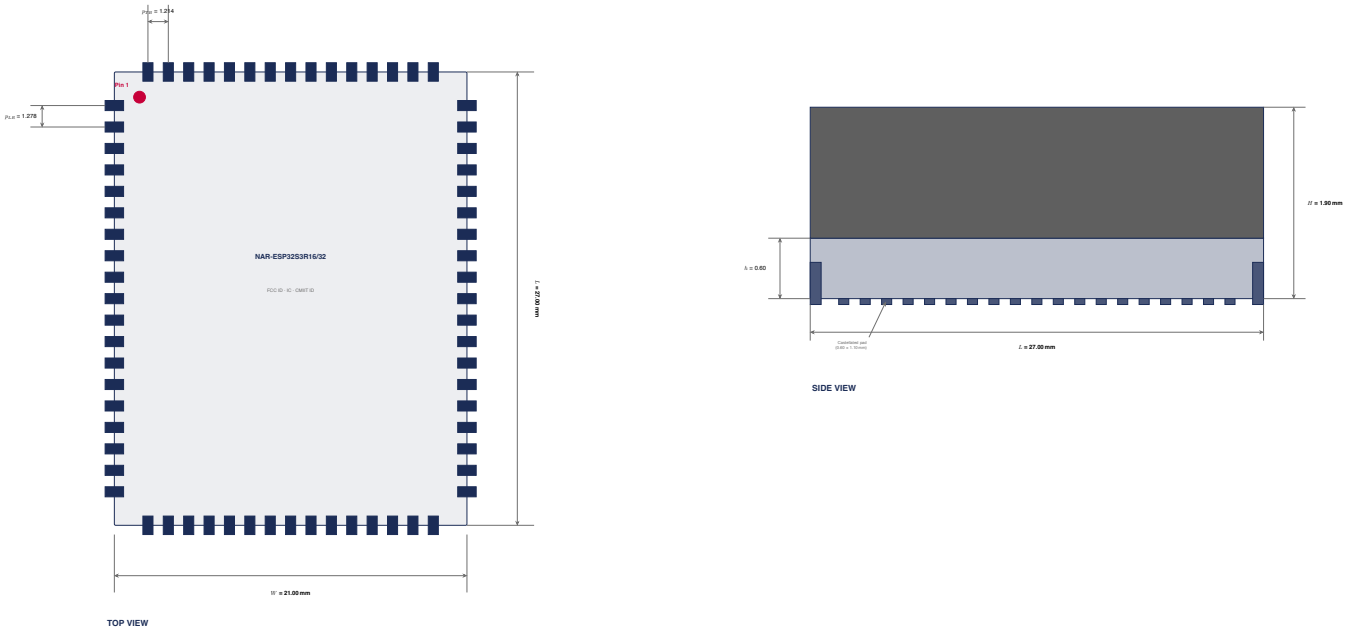

Figure 9.2. 2D mechanical drawing: top view with outer dimensions (L, W, pad pitches p_{LR}, p_{TB}) and the Pin 1 marker; side view with height (H), substrate thickness (h) and castellated pad detail. All dimensions in millimetres.

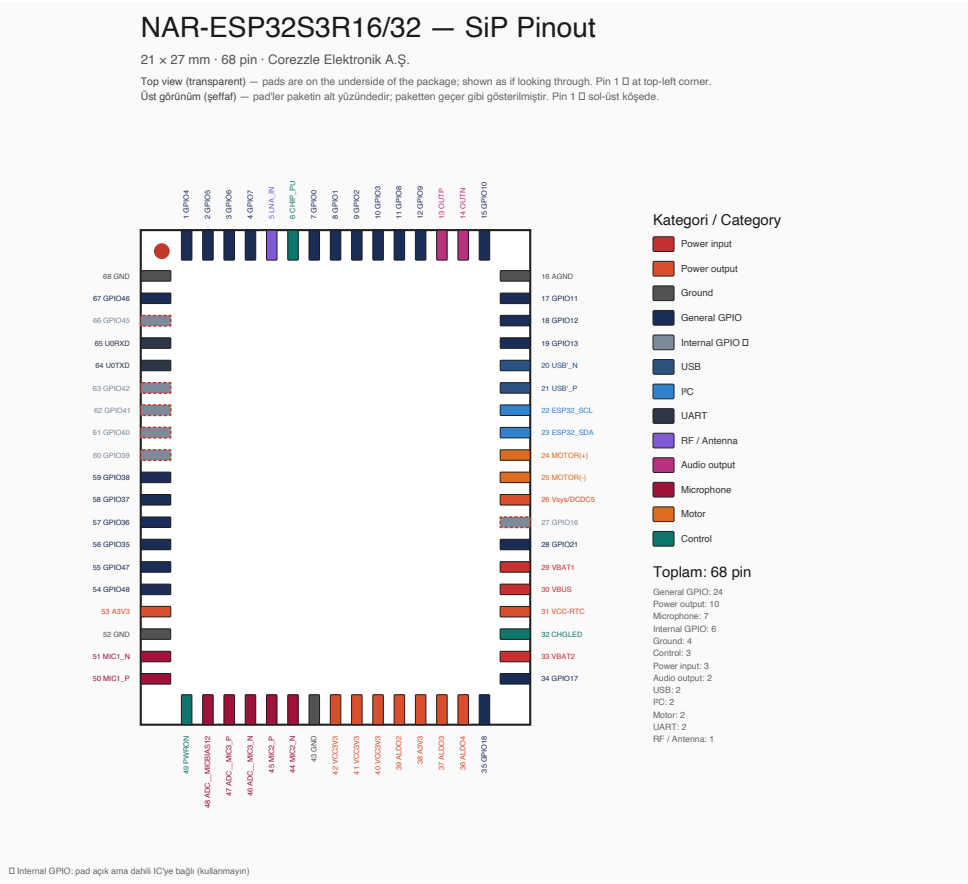

Figure 9.3. Top view (transparent). Colors indicate pin category.

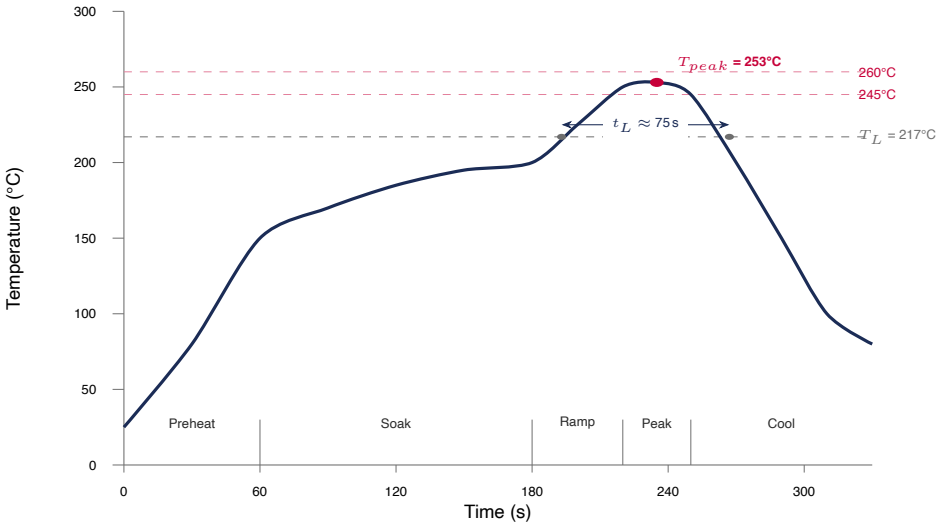

Figure 9.4. Recommended lead-free reflow profile — *typical recommendation profile*, J-STD-020E Table 4-2 (SAC305, $T_L = 217$ °C). Preheat ramp (≤ 3 °C/s), soak (60–120 s @ 150–200 °C), reflow ramp (≤ 3 °C/s), peak (245–260 °C, 10–30 s), time above liquidus ($t_L \leq 90$ s), cooling (≤ 6 °C/s). The specific point values in the graph (253 °C peak, ≈ 75 s above liquidus) are illustrative; the actual bench profile will be added after MSL3 qualification.

CHAPTER 10

Application Information

10.1 Reference Design

Figure 10.1 shows the minimum working external component count for NAR-ESP32S3R16/32. Charge IC, rail LDOs/bucks, crystals and decoupling are already integrated inside the SiP; only the following items are required on the external PCB:

- USB-C connector (5.1 kΩ pull-downs on CC1/CC2)
- Li-Ion/LiPo battery connector (JST-PH or similar)
- NTC thermistor (10 kΩ @25 °C, β=3950) on the TS pin, for battery thermal protection
- Antenna: PCB trace antenna or u.FL/IPEX connector (selected by pin configuration)
- Application-specific I/O connectors (LCD, touch, sensor)

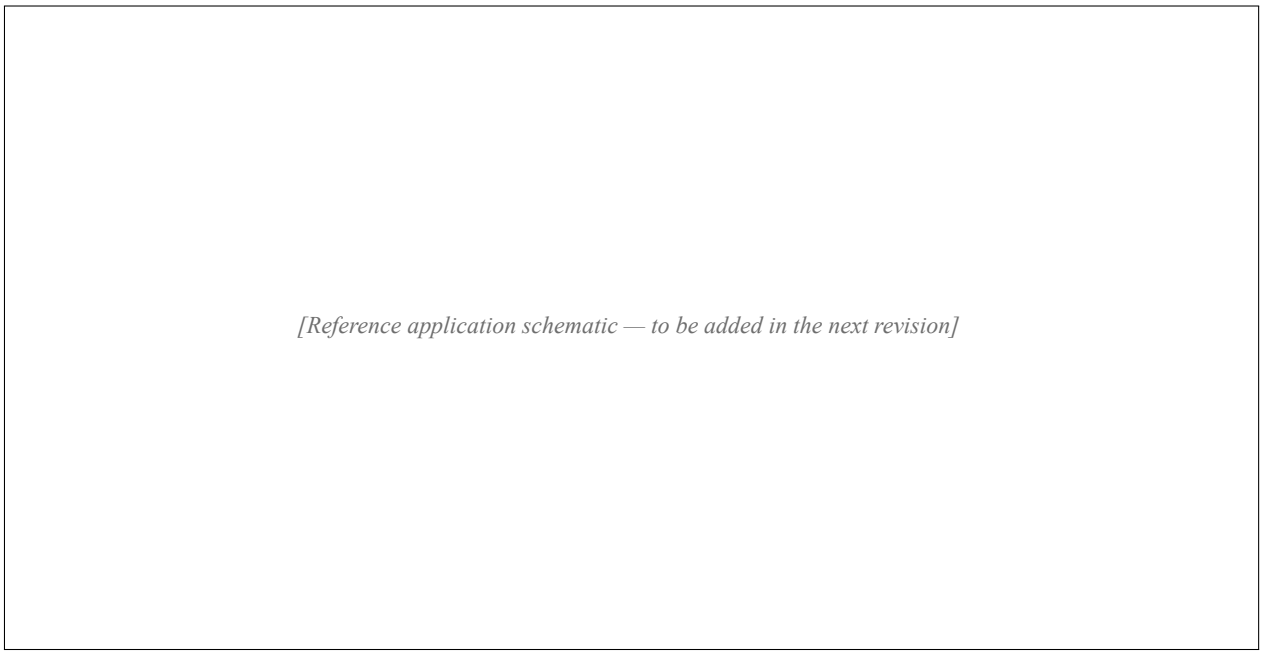

Figure 10.1. Typical application — minimum external circuit.

TBD (The complete reference schematic will be published in the next revision.)

10.2 Power — External BoM

Note: Decoupling capacitors for every on-package chip are *integrated within the package*; external decoupling is *not required* but improves transient performance.

Table 10.1. Recommended external power components.

Component	Description	Typical value
C_{VBUS}	Bulk cap on VBUS input (near USB plug)	10 µF + 100 nF X7R
C_{VBAT}	Transient cap on VBAT pin	100 µF tantalum/POLY + 100 nF X7R
C_{user}	User rail output (DCDC2–5 accessible)	22 µF + 100 nF X7R
$R_{CC1/CC2}$	USB-C CC pull-down (5.1 kΩ)	5.1 kΩ ±1%
R_{NTC}	Thermistor (on TS pin)	10 kΩ, β=3950
ESD/EMI filter	Optional, on connector lines	TVS + ferrite

10.3 Antenna Placement Guidelines

10.3.1 On-Package PCB Antenna (Default)

NAR-ESP32S3R16/32 ships with an on-package PCB antenna. For optimal RF performance, follow these guidelines on the host PCB:

- **Antenna clearance zone:** a 15 × 10 mm copper-free area around the antenna side of the package (on top and bottom layers, as well as adjacent inner layers).
- **GND plane:** no large solid GND plane should sit *beneath* or *beside* the antenna zone.
- **Metal chassis clearance:** keep at least 10 mm between the antenna side and any metal chassis or battery cell.
- **Human body (wearable):** wrist, arm and torso contact can affect RF performance by −2 to −5 dB; choose the antenna orientation carefully.

10.3.2 External u.FL / IPEX MHF1

When the RF output is routed to an external u.FL connector through pin configuration:

- **Impedance:** 50 Ω controlled microstrip or coplanar waveguide
- **Trace length:** 2 – 30 mm range, reflection ≤ −10 dB
- **Antenna choice:** 2.4 GHz band, ≥ 0 dBi gain recommended
- **Re-certification:** an externally-antennaed version requires a separate CE/FCC assessment

10.4 Decoupling Strategy

Decoupling capacitors for every on-package chip are *integrated within the package* (ESR and frequency response optimised at the factory). External capacitors on the host PCB are optional but follow good design practice:

- **Bulk:** 22 µF (X7R MLCC or tantalum) near every user rail pin
- **High frequency:** 100 nF (X7R) in parallel
- **Placement:** ≤ 5 mm from the pin, vias direct to GND plane

10.5 Thermal Considerations

NAR-ESP32S3R16/32 dissipates significant thermal power during RF TX and sustained Wi-Fi traffic. Recommended PCB measures:

TBD (Thermal resistance values θ_{JA} (junction-to-air) and θ_{JC} (junction-to-case) will be added following bench measurement.)

Table 10.2. Thermal design recommendations.

Measure	Description
Thermal via array	Minimum 4×4 grid beneath the package, 0.3 mm vias on 0.8 mm pitch
Bottom GND plane	Solid copper of at least 20×20 mm beneath the package
Multiple GND pad ties	Every GND pin tied directly to the PCB GND plane via vias
Airflow	Natural convection sufficient; no active cooling required ($T_a \leq +85$ °C)

10.6 EMI / EMC Guidance

Because NAR-ESP32S3R16/32 includes on-package RF calibration and EMI suppression filters, no additional measures are usually needed in the end product. Nonetheless:

- Optional common-mode choke (BLM21, BLM18 series) on USB-C lines
- Ferrite bead on high-speed signals with long PCB traces
- 2.5 mm guard ring (GND vias) around connectors

10.7 Software Development

The official open-source development kit for NAR-ESP32S3R16/32 (Apache-2.0):

- Repo: `https://github.com/CorezzleElectronics/nar-esp32s3-devkit`
- Frameworks: ESP-IDF v5.x (recommended), Arduino-ESP32, MicroPython, NuttX
- RTOS examples: FreeRTOS (default), Zephyr, NuttX
- Reference applications:
  - Smartwatch (UI, sensor fusion, BLE peripheral)
  - Vehicle tracker (optional GNSS, BLE/Wi-Fi telematics)
  - Voice IoT (wake-word, beamforming, Bluetooth audio)
  - Home automation (Wi-Fi gateway, BLE Mesh)
- Drivers: AXP2101, ES8311, ES7210, ICM-42670, PCF85063, GD25LQ256 (ESP-IDF managed component)
- Manufacturing test firmware: automated functional test via GitLab CI

CHAPTER 11

Ordering Information

11.1 Available Part Numbers

Table 11.1. Valid part numbers — production versions.

Part Number	Description	Packaging	MOQ
NAR-ESP32S3R16/32-LGA68	16 MB PSRAM + 32 MB flash, standard version	Tray	**TBD**
NAR-ESP32S3R16/32-LGA68-TR	Same, tape & reel packaging	T&R 13″	**TBD**
NAR-ESP32S3R16/32-EVB	Evaluation board (NAR-ESP32S3 + USB-C + battery connector + break-out)	—	1

TBD (MOQ values will be updated together with the production plan. Expected values: Tray ≤ 100, T&R 1 reel (per-reel count depending on reel size).)

11.2 Part Number Structure

NAR -- ESP32S3R16/32 -- LGA68 -- TR

Family MCU + Memory Package Packaging

Table 11.2. Part number field definitions.

Field	Possible value	Meaning
Family	NAR	Corezzle SiP product family
MCU + Memory	ESP32S3R16/32	ESP32-S3R16V (16 MB PSRAM) + 32 MB QSPI flash
Package	LGA68	LGA-68, castellated, 27×21 mm
Packaging	(empty)	Tray (default)
	TR	Tape & reel, EIA-481, 13″ (330 mm) reel
	EVB	Evaluation board (development kit)

11.3 Samples and Evaluation

11.3.1 Engineering Samples

Engineering samples and evaluation boards (NAR-ESP32S3-EVB) can be obtained via:

info@corezzle.com

Providing the following information when requesting samples helps expedite the process:

- Company name and application area
- Estimated annual volume (parts/year)
- Target market (TR / EU / US / other)
- NDA requirement (if any)

11.3.2 Development Kit

The NAR-ESP32S3-EVB evaluation board provides everything needed to test the device directly:

- NAR-ESP32S3R16/32 SiP (board centerpiece)
- USB-C connector (programming + power)
- Li-Ion battery connector (JST-PH 2-pin)
- Reset and boot buttons
- $0.1''$ pitch breakout headers for every SiP pin
- NTC thermistor (battery thermal protection)
- LEDs (status, charge, user)

Associated open-source software repository:
`https://github.com/CorezzleElectronics/nar-esp32s3-devkit`

11.4 Lead Time

Table 11.3. Typical lead times (approximate).

Type	Description	Lead time
Engineering sample	1–10 units, $\leq$ 2 weeks advance notice	1–2 weeks
Evaluation board (EVB)	1–10 units	1–2 weeks
Production sample	$\leq$ 1,000 units	**TBD** weeks
Mass production (1k–10k)	—	**TBD** weeks
Mass production ($>$ 10k)	—	**TBD** weeks

TBD (Production-scale lead times will be updated after contract signature and the production plan is finalized.)

11.5 Quality and Test

Every NAR-ESP32S3R16/32 unit passes an automated functional test (ATE) at the end of manufacturing:

- Voltage verification of all rails ($\pm$2% tolerance)
- ESP32-S3 boot + flash read/write test
- Wi-Fi + BLE TX/RX test (against calibrated reference)
- I^2C command test (PMIC, codec, mic ADC, IMU, RTC all respond)
- I^2S audio loopback (codec $\rightarrow$ mic ADC)

- USB-C enumeration test
- Test log stored together with the unit serial number

11.6 Warranty

NAR-ESP32S3R16/32 is delivered with a **12-month** warranty against manufacturing defects. The warranty does not cover damage caused by the user (ESD, over-voltage, mechanical damage). For detailed warranty terms, refer to the Corezzle sales agreement.

CHAPTER 12

Revision History

12.1 Revision Table

Table 12.1. Document revision history.

Revision	Date	Status	Changes
0.1	2026-05-16	Advance Information	Initial release. System architecture, on-package chip list, block diagram, 68-pin function table, AXP2101 rail mapping, peripheral performance tables (manufacturer nominal). Fields for electrical characterization and certification numbers are marked TBD.
0.2	2026-05-20	Advance Information	English edition added (parallel `sections-en/` tree and `main-en.tex`); shared `style/datasheet.sty` with TR/EN language switch.

12.2 Revision Levels

The NAR-ESP32S3R16/32 datasheet progresses through the following maturity levels. The current version is **Rev. 0.1 ADVANCE INFORMATION**.

Table 12.2. Datasheet revision levels.

Level	Definition	Target
Advance Information	Architecture, nominal values and reference circuit are published. Electrical measurement results are not yet included. Suitable for design planning and evaluation; *requires pre-production verification*.	Current
Preliminary	Bench characterization complete; typical electrical values, power consumption profiles and RF parameters updated with measured results. Certification numbers pending.	**TBD**
Final (Rev. 1.0)	Includes all electrical characterization, antenna measurements, mechanical tolerances and regulatory certification numbers (CE, FCC, IC, MIC, Bluetooth SIG). Release-ready for production and mass shipping.	**TBD**

12.3 Expected in the Next Revision

- Wi-Fi / BLE TX output power and RX sensitivity (measured typical values, ±tolerance)
- Measured typical / max values for all power consumption modes (modem-sleep, light-sleep, deep-sleep, hibernation)
- Antenna gain and radiation pattern
- Thermal resistance values (θ_{JA}, θ_{JC})
- Power-up timing diagram (rail ramp times, EN deassert delay)
- Full land pattern drawing
- Reference application schematic

12.4 Update Notification

To receive notifications when new revisions are published:

info@corezzle.com

Each datasheet page footer shows the current revision number (Rev. 0.1 ADVANCE INFORMATION); for the most up-to-date version, check corezzle.com.

CHAPTER 13

Legal and Compliance

13.1 Disclaimer

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13.2 Validity of Information

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13.12 Recycling and RoHS

NAR-ESP32S3R16/32 is compliant with RoHS 3 (2015/863/EU). At end of life, the product must be delivered to authorised recycling facilities in accordance with the Waste Electrical and Electronic Equipment (WEEE) regulations.

13.13 Contact

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CHAPTER 14

Upstream Datasheets

This datasheet provides *SiP-specific* integration information for the chips inside the package. The full electrical, timing and application datasheet for each chip should be obtained from its manufacturer. The table below lists direct source links.

14.1 Chip Datasheets

Espressif — ESP32-S3R16V

https://www.espressif.com/sites/default/files/documentation/esp32-s3_datasheet_en.pdf

X-Powers — AXP2101

https://github.com/CinaryEmbedded/AXP2101-Datasheet

Everest Semiconductor — ES8311 (audio codec)

https://www.everest-semi.com/pdf/ES8311DS.pdf

Everest Semiconductor — ES7210 (mic ADC)

https://www.everest-semi.com/pdf/ES7210DS.pdf

TDK InvenSense — ICM-42670-P

https://invensense.tdk.com/en-us/products/6-axis/icm-42670-p

NXP — PCF85063ATL

https://www.nxp.com/docs/en/data-sheet/PCF85063A.pdf

GigaDevice — GD25LQ256DWIGR

https://www.gigadevice.com/datasheet/gd25lq256e/

STMicroelectronics — USBLC6-2SC6

https://www.st.com/resource/en/datasheet/usblc6-2.pdf

14.2 Related Espressif Documents

ESP32-S3 Technical Reference Manual

https://www.espressif.com/sites/default/files/documentation/esp32-s3_technical_reference_manual_en.pdf

ESP32-S3 Hardware Design Guidelines

https://docs.espressif.com/projects/esp-idf/en/latest/esp32s3/hw-reference/

ESP-IDF Programming Guide

https://docs.espressif.com/projects/esp-idf/en/latest/esp32s3/

14.3 Standards and Regulations

- IEEE 802.11-2020 — Wireless LAN Medium Access Control
- Bluetooth Core Specification 5.0
- EN 300 328 v2.2.2 — Wideband transmission systems (2.4 GHz)
- FCC Part 15 Subpart C (15.247) — Intentional Radiators
- J-STD-020E — Moisture/Reflow Sensitivity Classification
- IPC-7351B — Generic Requirements for Surface Mount Design

14.4 Corezzle Documents

- **NAR-ESP32S3 Pinmap (TR)** — `docs/pinmap-tr.md`
- **NAR-ESP32S3 Onepager (TR)** — `docs/onepager-tr.md`
- **Development Kit** — https://github.com/CorezzleElectronics/nar-esp32s3-devkit